Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An input buffer receiver comprising:

a buffer input portion for receiving an input signal ~~SIGNAL_IN~~, said buffer input portion comprising a bias node;

a large capacitor ~~capacitance~~ between ~~a PMOS~~ the bias node and a ~~VSS source~~ lower supply voltage said large capacitor providing a coupling ratio between said large capacitor and a parasitic capacitor coupled between said bias node and a ground reference point approaching a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of a ground noise signal between the lower supply voltage and the ground reference point; and

a buffer output portion in communication with the buffer input portion for producing an output signal ~~SIGNAL_OUT1~~.

2. (Currently Amended) The input buffer receiver of claim 1, wherein the buffer input portion which receives ~~an~~ the input signal ~~SIGNAL_IN~~ further comprises:

a first transistor of a first conductivity type ~~N11~~ having a source node to which a ~~VSS source~~ the lower supply voltage is applied, a gate node to which a reference voltage ~~VREF~~ is applied, and a drain node at which the biasing voltage is developed ~~to which a signal VB11 is applied~~;

a second transistor of a second conductivity type ~~P11~~ having a drain node which is connected to the drain node of the first transistor ~~N11~~, and a gate node at which the biasing voltage is developed ~~to which a signal VB11 is applied~~, and a source node to which an upper supply voltage source ~~VDD~~ is applied;

a third transistor of the second conductivity type ~~P12~~ having a drain node which is connected to the drain of a fourth transistor ~~N12~~, a gate node at which the biasing voltage is developed ~~to which a signal VB11 is applied~~, and a source node to which ~~an~~ the upper supply voltage source ~~VDD~~ is applied;

a fourth transistor of the first conductivity type ~~N12~~ having a source node to which a ~~VSS source~~ lower suppply voltage is applied, a gate node to which an input signal ~~SIGNAL_IN~~ is applied externally, and a drain node which is ~~the~~ an input to the buffer output portion.

3. (Currently Amended) The input buffer receiver of claim 2 ~~1~~, wherein the first and fourth transistors~~, N11 and N12,~~ are NMOS transistors, and the second and third transistors~~, P11 and P12,~~ are PMOS transistors.

4. (Currently Amended) The input buffer receiver of claim 2 ~~1~~, wherein the large capacitor ~~capacitance~~ is connected between the sources of the first and fourth transistors~~, N11 and N12,~~ of the buffer input portion and the gate of the second transistor ~~P11~~ of the buffer input portion.

5. (Currently Amended) The input buffer receiver of claim 2 ~~1~~, wherein the gate of the second transistor ~~P11~~ is connected to its drain.

6. (Currently Amended) The input buffer receiver of claim 2 ~~1~~, wherein the gate of the second transistor ~~P11~~ is connected to the drain of the first transistor ~~N11~~.

7. (Currently Amended) The input buffer receiver of claim 2 ~~1~~, wherein the gate of the second transistor ~~P11~~ is connected to the gate of the third transistor ~~P12~~.

8. (Currently Amended) The input buffer receiver of claim 2 ~~1~~, wherein the buffer output portion which produces ~~an~~ output signal ~~SIGNAL_OUT1~~ comprises: a first inverter ~~I11~~ connected to the drain of the third transistor ~~P12~~ and the drain of the fourth transistor ~~N12~~;

9. (Currently Amended) The input buffer receiver of claim 2 ~~1~~, wherein ~~P12 and N12~~ the third transistor and the fourth transistor activate almost simultaneously to ~~provide an efficient circuit design technique for filtering~~ minimize the effects of ground noise on a delay jitter factor of said input buffer.

10. (Currently Amended) The input buffer receiver of claim 1, ~~involving a large capacitance coupling ratio, which~~ wherein the large capacitor charge couples the ~~PMOS~~ bias node of the input buffer receiver to the ~~VSS source~~ lower supply voltage of the input buffer receiver and wherein a capacitance value of the large capacitor is selected by the formula:~~.~~

$$\frac{CHC}{Cp + CHC} \approx 1$$

where:

CHC is the capacitance value of the large capacitor, and

Cp is the capacitance value of the parasitic capacitor.

11. (Currently Amended) The input buffer receiver of claim 1, ~~involving a~~ wherein the capacitance value of the large capacitor relative to said

parasitic capacitor ~~capacitance coupling ratio, which~~ results in a quicker response time for the output signal ~~a SIGNAL_OUT1~~.

12. (New) An integrated circuit formed on a substrate comprising:

an input buffer receiver for receiving an input signal and connected to said distribution network, said input buffer comprising:

a buffer input portion for receiving the input signal, said buffer input portion comprising a bias node;

a large capacitor between the bias node and a lower supply voltage, said large capacitor providing a coupling ratio between said large capacitor and a parasitic capacitor coupled between said bias node and a ground reference point approaching a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of a ground noise signal between the lower supply voltage and the ground reference point ; and

a buffer output portion in communication with the buffer input portion for producing an output signal.

13. (New) The integrated circuit of claim 12, wherein the buffer input portion of the input buffer receiver further comprises:

a first transistor of a first conductivity type having a source node to which the lower supply voltage is applied, a gate node to which a reference voltage is applied, and a drain node at which the biasing voltage is developed ;

a second transistor of a second conductivity type having a drain node which is connected to the drain node of the first transistor, and a gate node at which the biasing voltage is developed, and a source node to which an upper supply voltage source is applied;

a third transistor of the second conductivity type having a drain node which is connected to the drain of a fourth transistor, a gate node at which the biasing voltage is developed, and a source node to which the upper supply voltage source is applied;

a fourth transistor of the first conductivity type having a source node to which lower supply voltage is applied, a gate node to which an input signal is applied externally, and a drain node which is an input to the buffer output portion.

14. (New) The integrated circuit of claim 13, wherein the first and fourth transistors are NMOS transistors, and the second and third transistors are PMOS transistors.

15. (New) The integrated circuit of claim 13, wherein the large capacitor is connected between the sources of the first and fourth transistorsof the buffer input portion and the gate of the second transistor of the buffer input portion.

16. (New) The integrated circuit of claim 13, wherein the gate of the second transistor is connected to its drain.

17. (New) The integrated circuit of claim 13, wherein the gate of the second transistor is connected to the drain of the first transistor.

18. (New) The integrated circuit of claim 13, wherein the gate of the second transistor is connected to the gate of the third transistor.

19. (New) The integrated circuit of claim 13, wherein the buffer output portion which produces output signal comprises: a first inverter connected to the drain of the third transistor and the drain of the fourth transistor;

20. (New) The integrated circuit of claim 13, wherein the third transistor and the fourth transistor activate almost simultaneously to minimize the effects of ground noise on a delay jitter factor of said input buffer.

21. (New) The integrated circuit of claim 12, wherein the large capacitor charge couples the bias node of the input buffer receiver to the lower supply voltage of the input buffer receiver and wherein a capacitance value of the large capacitor is selected by the formula:

$$\frac{CHC}{Cp + CHC} \approx 1$$

where:

CHC is the capacitance value of the large capacitor, and

Cp is the capacitance value of the parasitic capacitor.

22. (New) The integrated circuit of claim 12, wherein the capacitance value of the large capacitor relative to said parasitic capacitor results in a quicker response time for the output signal.

23. (New) A method for minimizing effects of ground noise on an input buffer receiver comprising the steps of:

forming a buffer input portion for receiving an input signal on a substrate;

forming a bias node within said buffer input portion;

connecting said a lower supply voltage to said buffer input portion;

forming a large capacitor between the bias node and the lower supply voltage said large capacitor providing a coupling ratio between said large capacitor and a parasitic capacitor coupled between said bias node and a ground reference point approaching a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of a ground noise signal between the lower supply voltage and the ground reference point; and

forming a buffer output portion on said substrate in communication with the buffer input portion for producing an output signal.

24. (New) The method of claim 23, wherein forming the buffer input portion further comprises the steps of:

forming a first transistor of a first conductivity type on said substrate;

applying the lower supply voltage to a source node of the first transistor;

applying a reference voltage to a gate node of the first transistor;

connecting a drain node of the first transistor to develop as biasing voltage at said drain node;

forming a second transistor of a second conductivity type on said substrate;

connecting a drain node of the second transistor to the drain node of the first transistor;

connecting a gate node of the second transistor to the drain node of the first transistor for developing the biasing voltage; and

connecting a source node of the second transistor to an upper supply voltage;

forming a third transistor of the second conductivity type on said substrate;

connecting a drain node of the third transistor to the drain of a fourth transistor;

connecting a gate node of the third transistor to the drain node of the first transistor for developing the biasing voltage;

connecting a source node of the third transistor to the upper supply voltage source;

forming a fourth transistor of the first conductivity type on said substrate;

connecting a source node of the fourth transistor to the lower supply voltage;

connecting a gate node of the fourth transistor to receive an input signal externally; and

connecting a drain node of the fourth transistor to an input to the buffer output portion.

25. (New) The method of claim 24, wherein the first and fourth transistors are NMOS transistors, and the second and third transistors are PMOS transistors.

26. (New) The method of claim 24, wherein forming the large capacitor comprises the step of:

connecting said large capacitor between the sources of the first and fourth transistors of the buffer input portion and the gate of the second transistor of the buffer input portion.

27. (New) The method of claim 24, wherein forming the buffer input portion further comprises the steps of:

connecting the gate of the second transistor to its drain.

28. (New) The method of claim 24, wherein forming the buffer input portion further comprises the steps of:

connecting the gate of the second transistor to the gate of the third transistor.

29. (New) The method of claim 24, wherein forming the buffer output portion which produces output signal comprises the step of:

forming a first inverter on said substrate; and

connecting an input of said first inverter to the drain of the third transistor and the drain of the fourth transistor;

30. (New) The method of claim 24, wherein the third transistor and the fourth transistor activate almost simultaneously to minimize the effects of ground noise on a delay jitter factor of said input buffer.

31. (New) The method of claim 23, wherein the large capacitor charge couples the bias node of the input buffer receiver to the lower supply voltage of the input buffer receiver and wherein a capacitance value of the large capacitor is selected by the formula:

$$\frac{CHC}{Cp + CHC} \approx 1$$

where:

CHC is the capacitance value of the large capacitor, and

Cp is the capacitance value of the parasitic capacitor.

32. (New) The method of claim 23, wherein the capacitance value of the large capacitor relative to said parasitic capacitor results in a quicker response time for the output signal.

33. (New) An apparatus for minimizing effects of ground noise on an input buffer receiver comprising:

means for forming a buffer input portion for receiving an input signal on a substrate;

means for forming a bias node within said buffer input portion;

means for connecting said a lower supply voltage to said buffer input portion;

means for forming a large capacitor between the bias node and the lower supply voltage said large capacitor providing a coupling ratio between said large capacitor and a parasitic capacitor coupled between said bias node and a ground reference point approaching a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of a ground noise signal between the lower supply voltage and the ground reference point; and

means for forming a buffer output portion on said substrate in communication with the buffer input portion for producing an output signal.

34. (New) The apparatus of claim 23, wherein forming the buffer input portion further comprises:

means for forming a first transistor of a first conductivity type on said substrate;

means for applying the lower supply voltage to a source node of the first transistor;

means for applying a reference voltage to a gate node of the first transistor;

means for connecting a drain node of the first transistor to develop as biasing voltage at said drain node;

means for forming a second transistor of a second conductivity type on said substrate;

means for connecting a drain node of the second transistor to the drain node of the first transistor;

means for connecting a gate node of the second transistor to the drain node of the first transistor for developing the biasing voltage; and

means for connecting a source node of the second transistor to an upper supply voltage;

means for forming a third transistor of the second conductivity type on said substrate;

means for connecting a drain node of the third transistor to the drain of a fourth transistor;

means for connecting a gate node of the third transistor to the drain node of the first transistor for developing the biasing voltage;

means for connecting a source node of the third transistor to the upper supply voltage source;

means for forming a fourth transistor of the first conductivity type on said substrate;

means for connecting a source node of the fourth transistor to the lower supply voltage;

means for connecting a gate node of the fourth transistor to receive an input signal externally; and

connecting a drain node of the fourth transistor to an input to the buffer output portion.

35. (New) The apparatus of claim 24, wherein the first and fourth transistors are NMOS transistors, and the second and third transistors are PMOS transistors.

36. (New) The apparatus of claim 24, wherein means for forming the large capacitor comprises:

means for connecting said large capacitor between the sources of the first and fourth transistors of the buffer input portion and the gate of the second transistor of the buffer input portion.

37. (New) The apparatus of claim 24, wherein means for forming the buffer input portion further comprises:

means for connecting the gate of the second transistor to its drain.

38. (New) The apparatus of claim 24, wherein means for forming the buffer input portion further comprises the steps of:

means for connecting the gate of the second transistor to the gate of the third transistor.

39. (New) The apparatus of claim 24, wherein means for forming the buffer output portion which produces output signal comprises:

means for forming a first inverter on said substrate; and

means for connecting an input of said first inverter to the drain of the third transistor and the drain of the fourth transistor;

40. (New) The apparatus of claim 24, wherein the third transistor and the fourth transistor activate almost simultaneously to minimize the effects of ground noise on a delay jitter factor of said input buffer.

41. (New) The apparatus of claim 23, wherein the large capacitor charge couples the bias node of the input buffer receiver to the lower supply voltage of the input buffer receiver and wherein a capacitance value of the large capacitor is selected by the formula:

$$\frac{CHC}{Cp + CHC} \approx 1$$

where:

CHC is the capacitance value of the large capacitor CHC, and

Cp is the capacitance value of the parasitic capacitor Cp.

42. (New) The apparatus of claim 23, wherein the capacitance value of the large capacitor relative to said parasitic capacitor results in a quicker response time for the output signal.